

AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to Figs. 1-3.

Attachment: Replacement sheets

REMARKS

Claims 1 and 4-12 are pending in the present application. Claims 1 and 4-12 have been amended as a result of this response. Claims 2 and 3 have been canceled and no new claims have been added as a result of this response. Applicants respectfully submit that independent claims 1, 4, 9 and 11-12 and dependent claims 5-8 and 10 stand in condition for allowance.

I. Drawing Objections

The Examiner has objected to the drawings, stating that Figures 1-3 should be labeled by a legend such as --Prior Art-- .

In order to address this objection, Applicants respectfully submit that the suggestion in MPEP § 608.02(g) of the use of the phrase --Prior Art-- does not exclude the use of alternate phrases, for example, "Background Art" and "Related Art". These alternative phrases may be found in many U.S. Patents issued today. The intent of MPEP § 608.02(g) is to distinguish Applicants' invention from that which is not Applicants' invention. If a drawing figure illustrates only material which is known to be statutory prior art to the invention, then the use of the phrase --Prior Art-- in the drawing figure would be proper. However, if it is not clear whether such material is statutory prior art, then the use of the phrase --Prior Art-- in the drawing figures would not be proper, and a label such as "Background Art" or "Related Art" would be more appropriate.

Applicants are submitting drawing changes to Figs. 1-3 which include the label "Related Art" and respectfully submit that these amended drawings meet the criteria of MPEP § 608.02(g) and are sufficient to distinguish Applicants' invention from that which is not Applicants' invention. Accordingly, reconsideration and withdrawal of this objection, and approval of the proposed drawing corrections filed herewith, are respectfully requested.

II. Claim Rejections Under 35 U.S.C. § 112, second paragraph

The Examiner has rejected claims 4-8, 10 and 12 under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between elements. Claims 4-8, 10 and 12 have been amended to remove instances

referencing a second field-effect transistor. Therefore, this rejection is moot. Applicants respectfully request withdrawal of this rejection.

The Examiner has rejected claims 4-8, 10 and 12 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 4-8, 10 and 12 have been amended to correct the antecedent basis. Therefore, this rejection is moot. Applicants respectfully request withdrawal of this rejection.

III. Claim Rejections Under 35 U.S.C. § 102(b)

The Examiner has rejected claims 1-3 and 9 under 35 U.S.C. § 102(b) as being anticipated by Nakahara et al. (U.S. Patent No. 5,485,130) or Matsunaga et al. (U.S. Patent No. 4,789,846). These rejections are respectfully traversed. Claims 2 and 3 have been canceled and therefore this rejection is moot with respect to these claims.

Nakahara discloses a number of different switch circuits. For example, Figure 1 discloses a SPDT switch, however, the field-effect transistors are neither connected in parallel nor connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch. Figure 7 discloses a switch in which two field-effect transistors separated by a transmission line (14). Therefore, Figure 7 fails to disclose parallel field-effect transistors. In addition, Figure 7 fails to disclose field-effect transistors in which the inputs of the field-effect transistors are connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch.

Matsunaga discloses a number of different semiconductor switches. For example, Figure 6 discloses a SPDT switch, however, the field-effect transistors are neither connected in parallel nor connected directly between the input terminal of the SPST switch and the output terminal of the SPST switch. Figures 5(a), 5(b) and 6 disclose FET 14 and FET 38 which are *not directly* connected in parallel, rather, there is a one quarter wave length between drain 15 of FET 14 and drain 40 of FET 14 (Column 7, lines 46 to 56). Therefore, Matsunaga fails to disclose parallel field-effect transistors. In addition, Matsunaga fails to disclose field-effect transistors connected

directly between the input terminal of the SPST switch and the output terminal of the SPST switch.

Nakahara and Matsunaga fail to teach or disclose a SPST switch comprising “a plurality of field-effect transistor (FET) switches connected in parallel, each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor” and where “the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch” (claims 1 and 9).

Accordingly, for at least these reasons, claims 1 and 9 are clearly distinguishable over Nakahara in view of Matsunaga. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

IV. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1-8 and 10

The Examiner has rejected claims 1-8 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Tokumitsu et al. (JP 05-299995) in view of Nakahara et al. or Matsunaga et al. Applicants respectfully traverse the rejection in regards to claims 1 and 4-10.

Claims 2 and 3 have been canceled rendering the rejection moot.

Tokumitsu describes a microwave semiconductor switch that consists of two circuit portions in parallel with each other (Abstract and Figure 1). The first circuit portion consists of a switch in series with an inductor. The second circuit portion consists of a parallel circuit in series with a capacitor, the parallel circuit being a field-effect transistor in parallel with an inductor (Abstract and Figure 1). Therefore, Tokumitsu fails to disclose a SPST switch “between an input terminal and an output terminal, said SPST switch” constructed by “directly connecting an inductor in parallel with a series circuit, the series circuit consisting of a capacitor connected in series with a drain or source of a FET” (Claim 4).

Figure 6 of Tokumitsu discloses a SPDT switch. The SPDT switch of Tokumitsu has a parallel circuit in series with a capacitor, the parallel circuit being a gate in parallel with an inductor. Additionally, the parallel circuit in series with a capacitor is a first portion of a switch, which is in parallel with a second portion of a switch consisting of a gate in series with an

inductor. Tokumitsu fails to disclose a SPST switch comprising a “plurality of field-effect transistor (FET) switches connected in parallel, each of said plurality of FET switches having a field-effect transistor whose drain and source are directly connected in parallel with an inductor, wherein the input of said plurality of FET switches is directly connected to the input terminal of said SPST switch and the output of said plurality of FET switches is directly connected to the output terminal of said SPST switch” (claim 1). Claim 10 is allowable for similar reasons.

Nakahara or Matsunaga do not remedy the noted deficiencies of Tokumitsu. This reliance on Nakahara or Matsunaga fails to make up for the deficiencies of Tokumitsu discussed above with respect to independent claims 1 and 4. Therefore, the asserted combination of Tokumitsu and Nakahara or Matsunaga (assuming these references may be combined, which Applicants do not concede) fails to establish *prima facie* obviousness of any pending claim.

Accordingly, for at least these reasons, claims 1, 4 and 10 are clearly distinguishable over Tokumitsu in view of Nakahara or Matsunaga. Applicants submit that claims 5-8 are allowable at least by virtue of their dependency on claim 4. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claim 11

The Examiner has rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Nakahara et al. or Matsunaga et al. in view of Wallace et al. (U.S. Patent No. 6,137,377). Applicants respectfully traverse the rejection.

Wallace et al. does not remedy the noted deficiencies of Nakahara or Matsunaga. Wallace is only relied upon to allegedly teach a multiple-pole multiple throw switch. This reliance on Wallace fails to make up for the deficiencies of Nakahara or Matsunaga discussed above with respect to independent claims 1 and 4. Therefore, the asserted combination of Nakahara or Matsunaga and Wallace (assuming these references may be combined, which Applicants do not concede) fails to establish *prima facie* obviousness of any pending claim.

Accordingly, for at least these reasons, Applicants submit that claim 11 is allowable. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claim 12

The Examiner has rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Tokumitsu et al. in view of Nakahara et al. or Matsunaga et al. as applied to claim 4 and further in view of Wallace et al. Applicants respectfully traverse the rejection.

Wallace et al. does not remedy the noted deficiencies of Tokumitsu et al. in view of Nakahara et al. or Matsunaga. Wallace is only relied upon to allegedly teach a multiple-pole multiple throw switch. This reliance on Wallace fails to make up for the deficiencies of Nakahara or Matsunaga discussed above with respect to independent claims 1 and 4. Therefore, the asserted combination of Tokumitsu et al. in view of Nakahara et al. or Matsunaga and Wallace (assuming these references may be combined, which Applicants do not concede) fails to establish *prima facie* obviousness of any pending claim.

Accordingly, for at least these reasons, Applicants submit that claim 12 is allowable. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

V. Conclusion

All matters having been addressed in view of the foregoing, Applicants respectfully request the entry of this Amendment, the Examiner's reconsideration of this application, and the immediate allowance of all pending claims.

Applicants' undersigned representative remains ready to assist the Examiner in any way to facilitate and expedite the prosecution of this matter. If any point remains an issue in which the Examiner feels would be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

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Please charge any fees associated with the submission of this paper to Deposit Account No. 02-2448. The Commissioner for Patents is also authorized to credit any overpayments to the above-referenced deposit account.

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Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29,680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road

Suite 100 East

P.O. Box 747

Falls Church, Virginia 22040-0747

(703) 205-8000

Attorney for Applicants